REMARKS

Claims 28-51 remain in the present application. Claims 28, 30-31, 37, 39-40, 46 and 49 are amended herein. Applicants respectfully submit that no new matter has been added as a result of the claim amendments. Applicants respectfully request further examination and reconsideration of the rejections.

Claim Rejections – 35 U.S.C. §102

Claims 28-33, 35, 37-42, 44 and 46-50

Claims 28-33, 35, 37-42, 44 and 46-50 are rejected in the present Office Action under 35 U.S.C. §102(b) as being anticipated by United States Patent Number 3,805,247 to Zucker et al. (referred to herein as "Zucker"). Applicants respectfully submit that the embodiments of the present invention as recited in Claims 28-33, 35, 37-42, 44 and 46-50 are neither anticipated nor rendered obvious by Zucker for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 28, which recites a system comprising (emphasis added):

> a plurality of memory resources;
> a plurality of peripheral resources;
> a plurality of processors;
> a memory controller coupled to said plurality of processors and said plurality of memory resources, wherein said memory controller comprises a first resource controller for controlling access of said plurality of processors to said plurality of memory resources, wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor of said plurality of processors and a first memory resource of said plurality of memory resources, wherein said first resource controller is further operable to implement a second bus for enabling second communication between a second processor of said plurality of processors and a second memory resource of said plurality of memory resources, and wherein said first

resource controller is further operable to implement said first and second buses for enabling said first communication to occur independently of said second communication; and

a peripheral controller coupled to said plurality of processors and said plurality of peripheral resources, wherein said peripheral controller comprises a second resource controller for controlling access of said plurality of processors to said plurality of peripheral resources, and wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources.

Independent Claims 37 and 46 recite limitations similar to independent Claim 28. Claims 29-33, 35, 38-42, 44 and 47-50 depend from their respective independent Claims and recite further limitations to the claimed invention.

Applicants respectfully submit that Zucker fails to teach or suggest the limitations of "wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor of said plurality of processors and a first memory resource of said plurality of memory resources," "wherein said first resource controller is further operable to implement a second bus for enabling second communication between a second processor of said plurality of processors and a second memory resource of said plurality of memory resources" and "wherein said first resource controller is further operable to implement said first and second buses for enabling said first communication to occur independently of said second communication" as recited in independent Claim 28. As recited and described in the present application, a memory controller includes a first resource controller for controlling access of a plurality of processors to a plurality of memory resources. The first resource controller is further operable to implement a first bus for enabling first communication between a first processor of the plurality of processors and a first

memory resource of the plurality of memory resources. The first resource controller is further operable to implement a second bus for enabling second communication between a second processor of the plurality of processors and a second memory resource of the plurality of memory resources. The first resource controller is further operable to implement the first and second buses for enabling the first communication to occur independently of the second communication.

In contrast to the claimed embodiments, Applicants understand Zucker to teach a shared bus for enabling communication between a plurality of processors and a plurality of memory modules. For example, Zucker teaches output switch network (OSN) 84 for sending "data and address from a processor 10 to an addressed memory module 12," where "OSN 84 is a 'demultiplexer'" (col. 10, lines 55-60). Applicants respectfully submit that OSN 84 implements a shared bus since it is a demultiplexer and further since the processors are coupled to the memory modules through the demultiplexer. Therefore, Applicants respectfully submit that Zucker fails to teach or suggest two distinct buses (e.g., a first bus and a second bus) as claimed.

Additionally, Applicants fail to find any teaching or suggestion in Zucker of *independent* communication over a first and second bus as claimed. More specifically, Applicants fail to find any teaching or suggestion in Zucker of a first communication over the first bus (e.g., between a first processor and a first memory resource) occurring *independently* of a second communication over the

second bus (e.g., between a second processor and a second memory resource). Accordingly, Applicants reiterate that Zucker fails to teach or suggest the limitations of "wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor of said plurality of processors and a first memory resource of said plurality of memory resources," "wherein said first resource controller is further operable to implement a second bus for enabling second communication between a second processor of said plurality of processors and a second memory resource of said plurality of memory resources" and "wherein said first resource controller is further operable to implement said first and second buses for enabling said first communication to occur independently of said second communication" as recited in independent Claim 28.

Further, although page 2 of the rejection suggests that Zucker teaches two processors simultaneously accessing different memories, Applicants respectfully disagree. Applicants fail to find any teaching or suggestion in Zucker of two processors simultaneously accessing different memories as suggested by the rejection. Additionally, Zucker defines the term "parallel processing" to mean that more than one processor is available on a system (col. 12, lines 18-19). However, Zucker fails to teach or suggest that the two processors independently communicate over respective buses with respective memory resources as claimed. Accordingly, Applicants reiterate that Zucker fails to teach or suggest the limitations of "wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor

of said plurality of processors and a first memory resource of said plurality of memory resources," "wherein said first resource controller is further operable to implement a second bus for enabling second communication between a second processor of said plurality of processors and a second memory resource of said plurality of memory resources" and "wherein said first resource controller is further operable to implement said first and second buses for enabling said first communication to occur independently of said second communication" as recited in independent Claim 28.

For these reasons, Applicants respectfully submit that independent Claim 28 is neither anticipated nor rendered obvious by Zucker, thereby overcoming the 35 U.S.C. §102(b) rejection of record. Since independent Claims 37 and 46 recite limitations similar to those discussed above with respect to independent Claim 28, independent Claims 37 and 46 also overcome the 35 U.S.C. §102(b) rejection of record. Since dependent Claims 29-33, 35, 38-42, 44 and 47-50 recite further limitations to the invention claimed in their respective independent Claims, Applicants respectfully submit that Claims 29-33, 35, 38-42, 44 and 47-50 are also neither anticipated nor rendered obvious by Zucker. Therefore, Applicants respectfully submit that Claims 28-33, 35, 37-42, 44 and 46-50 are allowable.

Claim Rejections – 35 U.S.C. §103

Claims 34 and 43

Claims 34 and 43 are rejected in the present Office Action under 35 U.S.C. §103(a) as being unpatentable over Zucker in view of United States Patent Number 5,949,982 to Frankeny et al. (referred to herein as "Frankeny"). Applicants respectfully submit that the embodiments of the present invention as recited in Claims 34 and 43 are not rendered obvious by Zucker in view of Frankeny for the following reasons.

Applicants respectfully submit that Frankeny, either alone or in combination with Zucker, fails to cure the deficiencies of Zucker discussed herein. More specifically, Applicants respectfully submit that Frankeny also fails to teach or suggest the limitations of "wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor of said plurality of processors and a first memory resource of said plurality of memory resources," "wherein said first resource controller is further operable to implement a second bus for enabling second communication between a second processor of said plurality of processors and a second memory resource of said plurality of memory resources" and "wherein said first resource controller is further operable to implement said first and second buses for enabling said first communication to occur independently of said second communication" as recited in independent Claim 28, and similarly recited in independent Claim 37. Accordingly, independent Claims 28 and 37 are not rendered obvious by Zucker in view of Frankeny. Since dependent Claims

34 and 43 recite further limitations to the invention claimed in their respective independent Claims, Applicants respectfully submit that Claims 34 and 43 are also not rendered obvious by Zucker in view of Frankeny. Therefore, Applicants respectfully submit that Claims 34 and 43 are allowable.

Claims 36, 45 and 51

Claims 36, 45 and 51 are rejected in the present Office Action under 35 U.S.C. §103(a) as being unpatentable over Zucker. Applicants respectfully submit that the embodiments of the present invention as recited in Claims 36, 45 and 51 are not rendered obvious by Zucker for the following reasons.

Page 4 of the rejection takes official notice of the limitations "wherein said plurality of memory resources, said plurality of peripheral resources, said plurality of processors, said memory controller, and said peripheral controller comprise components of a portable electronic device" as recited in Claim 36, and similarly recited in Claims 45 and 51. Applicants respectfully disagree with this assertion and direct the Examiner to MPEP §2144.03(E), which states that "[i]t is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based." Additionally, as stated in MPEP §2144.03(C): "'[T]he Board [or examiner] must point to some concrete evidence in the record in support of these findings' to satisfy the substantial evidence test. If the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual

statements and explanation to support the finding." Accordingly, Applicants respectfully invite the Examiner to provide documentary evidence in the next Office Action if the rejection is to be maintained (see MPEP §2144.03(C); see 37 CFR §1.104(c)(2)).

Furthermore, Applicants respectfully submit that independent Claims 28, 37 and 46 are neither anticipated nor rendered obvious by Zucker for the reasons discussed herein. Since dependent Claims 36, 45 and 51 recite further limitations to the invention claimed in their respective independent Claims, Applicants respectfully submit that Claims 36, 45 and 51 are also not rendered obvious by Zucker. Therefore, Applicants respectfully submit that Claims 36, 45 and 51 are allowable.

CONCLUSION

Applicants respectfully submit that Claims 28-51 are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Dated: 2 / 17 / 2009 /BMF/

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